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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,810	07/10/2003	Mark E. Schuelein	1000-0011	2270

7590 06/29/2004

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,810	SCHUELEIN, MARK E.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 22-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-15 and 22-30* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response to the restriction/election requirement without traverse filed on 6/4/04 has been entered. In view of the further consideration, the species election requirement is withdrawn. The following is a detailed Office action of claims 1-15 and 22-30.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the digital processing device and the flash memory as recited in claim 27 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: the background of the invention section, the summary of invention section and their headers are missing.

Appropriate correction is required.

Claim Objections

4. Claim 7 is objected to because of the following informalities: the term "conventional" should be deleted to avoid potential 112, second paragraph problem because what is seen as conventional today may not be conventional tomorrow.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002

do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-7, 9-10, 13-15, 22-24 and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,433,601, issued to Ganesan.

As per claim 1, Ganesan discloses a flip-flop (Fig. 4), comprising:

a state retention portion (420) to store a bit of digital data (at nodes 401 and 402), having a first storage node (401) and a second storage node (402); and

a clocking portion (circuit 410, T1-T4) to transfer a new bit of digital data (DATA) to the state retention portion in response to a clock signal (CLK), the clocking portion including:

a first stack of transistors (T1 and T3) coupled to the first storage node (401) to function as recited, the first stack of transistors including a first transistor (T1) having a gate terminal coupled to receive said clock signal (CLK) and a second transistor (T3) having a gate terminal coupled to receive a delayed, inverted version of said clock signal (by the delayed, inverted circuit 410).

As per claim 2, the recited limitation is met as disclosed in column 5, line 56, i.e., N channel transistors, or in other words, N channel MOSFET, also see the specification of the present invention, page 3, line 16-17).

As per claim 3, Ganesan further discloses a second stack of transistors (T2 and T4) coupled to the second storage node (402) and functioned as recited, the second digital data value being different from said first digital data value (this is how a flip-flop is functioned), the second

stack of transistors including a third transistor (T2) having a gate terminal coupled to receive said clock signal and a fourth transistor (T4) having a gate terminal coupled to receive a delayed, inverted version of said clock signal.

As per claim 4, rejected for the same reason noted in claim 2.

As per claim 5, Fig, 4 clearly shows the connections of the gate terminals of T1-T4 as recited.

As per claim 6, the recited clock node reads on the node receive the clock CLK, the recited inversion device reads on the circuit 410.

As per claim 7, see the inverters in the circuit 410.

As per claims 9-10, the circuit 420 has only one latch having two inverters crossed coupled.

As per claim 13, the recited next state generation portion reads on transistors T5, T6 and inverter 430. Since the DATA signal is not part of the flip-flop, the DATA signal is seen as signal from an external source supplied to the flip-flop.

As per claim 14, the recited inversion device reads on inverter 430.

As per claim 15, the recited input node reads on the node receiving the DATA signal, the recited first inversion device reads on T5, i.e., the signal at the drain terminal of T5 is the inverted signal of the DATA signal.

As per claim 22, this claim is merely a method to operate a flip-flop having the structure discussed in claim 3, since Ganesan teaches the circuit, he inherently teaches the method.

As per claims 23-24 and 26, these claims are rejected for the same reasons noted in claims 6-7 and 10, respectively.

As per claim 27, this claim is rejected for the same reasons noted in claim 1. Further, because a flip-flop is a digital processing device, the recited digital processing device reads on the flip-flop itself. Ganesan teaches the flip-flop is used in with a MMX processor to replace prior art flip-flop (column 2, line 9), and it is clear that MMX processor is used in a computer system which includes flash memory, the limitation recited on the last line is met.

As per claims 28-30, the claims are rejected for the same reasons noted in claims 3, 6 and 9, respectively.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,433,601, issued to Ganesan.

As per claim 8, Ganesan discloses a flip-flop (shown in Fig. 6) having the same structure as discussed in claim 6 (Fig. 4) herein above wherein the inversion device includes a NAND gate having a first input terminal receives the clock signal CLK through a delay circuit D1, a second input terminal receives an enable signal (SCAN) through an inverter 415 and an output terminal provides output signal to the gate of the second transistor T3A through inverter 413A, but he does not explicitly disclose the inversion device include a NOR gate as called for in the claim.

However, as understood by a person skilled in the art, replacing the NAND gate 412a and inverter 413a by a NOR gate in the Ganesan circuit will give the same output logic to the gate of the second transistor T3A, i.e., art equivalent. recognized my 6/24/04

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Ganesan's (NAND gate 412a and inverter 413a) by a NOR gate for the motivation that to reduce the number of gate in the circuit.

As per claim 25, rejected for the same reason and motivation noted in claim 8.

Allowable Subject Matter

7. Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11-12 are allowable because the prior art of record fails to disclose or suggest the inclusion of first and second pull-up circuits connected as recited in claim 11.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/24/04

Minh Nguyen
Primary Examiner
Art Unit 2816